# Design and Development Of 10W SSPA For S Band MPAR

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***Abstract:***

***This paper describes the design and development of S-Band Solid State Power Amplifier with harmonic suppression, using Cree's CGH40010 .This SSPA is designed to operate in class-AB mode at 2.85 GHz and delivers 10 W pulsed power in S Band with an efficiency more than 60%.The matching circuitry designed by micro strip Transmission line and stubs using smith chart application tool, with a special consideration for suppressing the harmonics.***

***Key Words:S-Band SSPA,Stability analysis,Load pull analysis and matching,Harmonic suppression.***

## I. INTRODUCTION

This paper describes the design and fabrication aspects of 10 W Solid State Power Amplifier (SSPA) in S band using gallium nitride (GaN) **device**. This SSPA is intended to be a part of the Transmit Receive Module for S Band multifunction Phased Array Radar (MPAR) prototype. The design is carried out on FR4 substrate having dielectric constant(εr)4.5.

The device is biased in class AB to achieve better efficiency through transmission lines. Radial stubs also used in the bias circuitry to provide proper grounding at RF frequencies. The stability analysis is carried out and found that circuit is marginally stable. Marginally stable Device is stabilized using additional stabilization circuitry. Load pull technique is applied to find out the optimal load for maximizing delivered power. The matching circuitry designed by micro strip Transmission line and stubs using smith chart application tool, with a special consideration for suppressing the harmonics which ensure the amplifier is linear.

## II. BIASING NETWORK DESIGN

DC analysis were carried out to choose the bias point in class AB to achieve better efficiency. Gate and Drain Biasing Circuit designed by considering to stabilize the device in case a negative resistance appears in the gate at any frequency, to filter the signal, the products and the harmonics generated by the device from low to high frequencies without affecting the matching circuit. The impedance of bias circuit in parallel to the matching circuit is made infinite at the fundamental frequency by adding quarter- wavelength with different characteristic impedance according to the current requirement. A series of bypassing capacitors is used in the bias network to facilitate extended bypass frequency below the carrier in addition to a Radial shunt stub, it is designed at the 2.85 GHz as it creates a low impedance to the ground at a precise point and its physical length is shorter than the equivalent transmission line[1]. Blocking capacitors are selected from ATC 100A series because of its low ESR,low magnitude of impedance and the FSR is near to the design frequency with less tolerance.

## III. STABILITY ANALYSIS AND DESIGN OF STABILISATION CIRCUIT

Stability is one of the most important criteria's that should be considered in amplifier design. The amplifier circuit may be stable or potentially unstable. If it is potentially unstable, there are conditions where oscillations can occur. It is imperative that the amplifier does not oscillate in the product environment, since such behavior leads to product malfunction. Stability test is evaluated at all frequencies in-band and out-of-band of the circuit.

Stability test is carried out using stability circles, k- Δ , μ source/ load stability tests even one of these will be sufficient Result from simulations for stability was presented in figure 1.It is found that device is conditionally stabile at low frequency. In order to overcome this stability issue, a parallel connected RC circuit is attached to the gate side of the transistor. Minimum-loss stabilizing resistor of 33 ohm which is determined form stability circles [2] with a capacitor of 5.6 pF in parallel is used in the design.

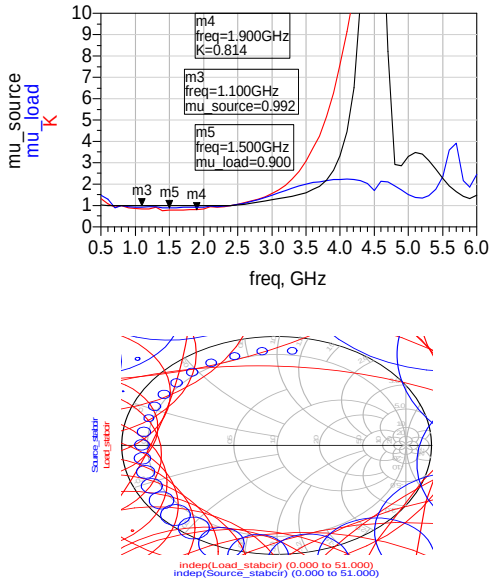


Fig.1 Stability analysis before stabilization K, μ factor and Load and source stability circles.

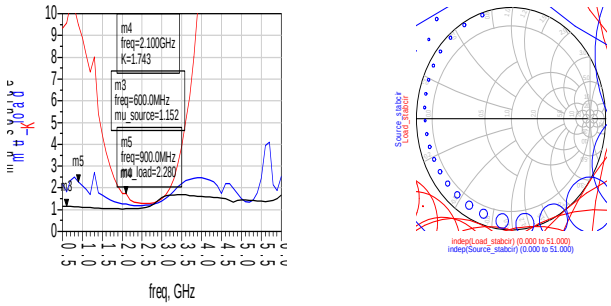


Fig.2 Stability analysis after stabilization K , μ factor and Load and source stability circles.

## IV. LOAD PULL ANALYSIS AND MATCHING NETWORK DESIGN

The performance of device is evaluated under different load conditions with the chosen bias point and input power for power amplifiers circuit. It were used to find power added efficiency and power delivered to the load for a range of load impedances. For this test, a large signal model CGH40010F from Cree is used. It is found that optimum load and source impedance are 10.79+j*2.29 and 2.95+j*1.35.

Matching network design is carried with optimum impedance found from load pull test. Matching is carried out by micro strip Transmission line and stubs using smith chart application tool .Harmonics are suppressed while designing matching network by changing the characteristic impedance of the stubs which ensure the amplifier is linear. The *Q* curves are used as guideline boundaries for broadband transformations [3] with an intermediate transformation of 50 ohm to 20 ohm by 31 ohm characteristic impedance line in both input and out put side.

## V. SIMULATION AND FABRICATION

1-Tone and 2-Tone Simulations are carried out for simulating the large-signal characteristics of the amplifier. These simulation results are presented in figure 3 . 600 MHz Bandwidth, 54% PAE(Power Added efficiency) ,14 dB Transducer power gain and harmonics better than 40 dBc is able to achive in simulation .

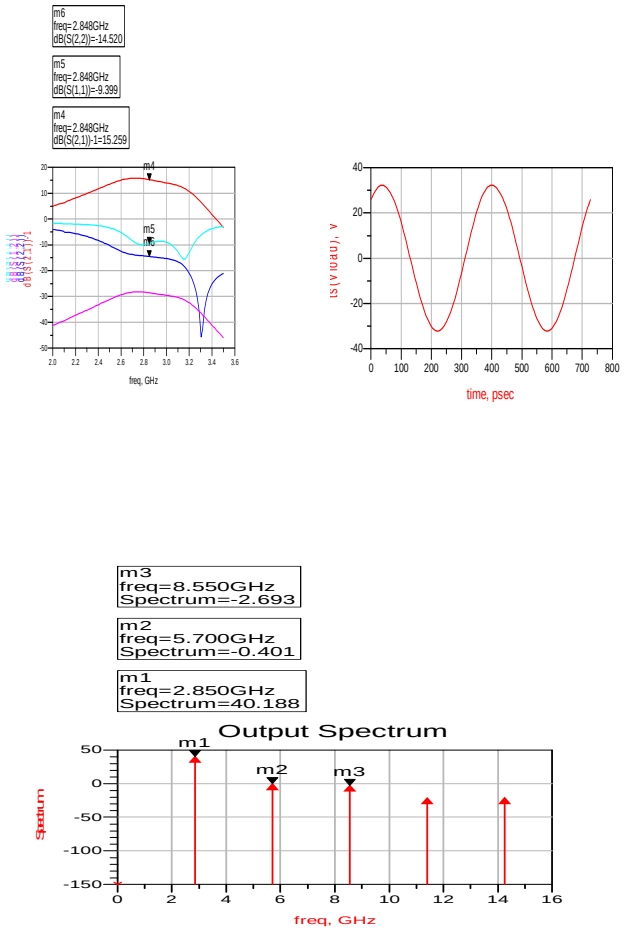


Fig.3 Harmonic Balance simulation and small signal gain.

Fabrication is carried out on FR-4 material having substrate height 0.2030 mm, conductor thickness 0.03048 mm dielectric constant(εr) 4.5 and a loss tangent of .035. Layout of final circuit is shown in figure 4.

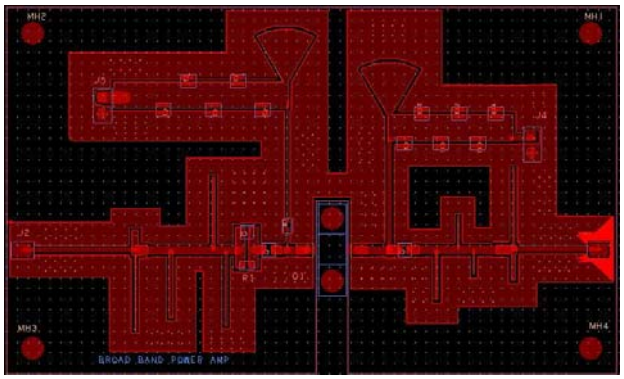


Fig. 4 Layout of S-band Power amplifier .

## CONCLUSION

Design and simulation of S-band Power amplifier is carried out. Simulation results were found satisfactory and PCB is fabricated. Realisation and testing of the amplifier circuit to be carried out.

## REFERENCES

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[3] Anthony J. Bichler "An ntroduction to Broadband Impedance Transformation for RF Power Amplifiers"

## BIODATA OF AUTHORS

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